

## **REMARKS**

In response to the Office Action mailed April 30, 2003, Applicant wishes to enter the following remarks for the Examiner's consideration. Claims 1-15 are currently pending in the Application as filed. Applicant has amended claims 1, 5, 6, 10 and 14.

### ***Disclosure***

The disclosure is objected to because of the use of "current potential" in the specification and claims. Applicant has amended independent claims 1, 10, and 14 to recite current. Applicant was not, however, able to find the use of this phrase in the specification and so it has not been amended.

### ***Claims Rejections***

Claims 5-9 are rejected as being indefinite. Claims 5 and 6 have been amended to overcome this rejection. Reconsideration and allowance of claims 5-9 is therefore earnestly solicited at the Examiner's earliest convenience.

Claims 1-4 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fattaruso. Applicant respectfully traverses this rejection of the claims. There are at least several claim recitations of the present invention that are not taught, disclosed, suggested or otherwise anticipated by the Fattaruso reference.

With regard to claims 1-4 and 14, the claim language recites that the input stage is suitable for accepting an input signal. In the Fattaruso reference, 10 is described as an input differential amplifier stage (emphasis added) since differential circuit DF1 accepts TWO input signals IN10 and IN11.

Also with regard to claims 1-4 and 14, the claim language states that the first and second output signals generated by the output stage are caused to have the same current by the current mirror configuration of the gain stage. In the Fattaruso reference, while current mirrors are used in the input differential amplifier stage 10

(CM1) and the feedforward stage (CM2), there is no teaching, disclosure or suggestion that a Indeed, column 4, line 67, to column 5, line 6 teaches that the current at node CN3 affects the channel conductances of transistors M23 (to which Mf1 is coupled) and M22 and thus “concurrently changes the amount of current passing through the ... M23 and the amount of current passing through .... M22.” The Examiner’s characterization of transistors Mf1 and M21 as producing output signals is incorrect; the reference teaches that Mf1 is part of the feedforward stage 12 – only transistor M21 of output stage 14 is coupled to output signal OUT. And, in fact, the Fattaruso reference only teaches the production of ONE output signal, OUT10 (shown as OUT) in FIG. 7, by output stage 14.

With regard to the input stage recitations of claim 2, it is recited that the control terminals of the first and second transistors of the input stage are coupled to receive the input signal. The Examiner asserts that transistors M11, M12 of FIG 7 of Fattaruso correspond to these transistors, but they do not, in fact, have their control terminals coupled together to receive an input signal, with the control terminal of each instead being coupled to its own input signal, IN10 and IN11, respectively. Moreover, the claim recites that the second terminals of the first and second transistors (those terminals not coupled to the current source) are coupled to the gain stage. In FIG. 7, it can be seen that the M11, M12 are NTO coupled to feedforward stage 12. Rather the terminals of these transistors I1, part of differential circuit DF1, not connected to current source are coupled to current mirror CM1, also described in Fattaruso as part of the input differential amplifier stage 10.

It is noted that claim 3 depends from claim 2.

With regard to claims 3 and 4, which both ultimately depend from claim 1, the second terminals of the transistors of the current mirror of the gain stage are not only coupled to a constant voltage source, they are coupled to the output stage of the current amplifier cell. This is not taught or suggested by Fattaruso in which the terminals of M13, M14 (suggested to be the transistors of the gain stage by the

Examiner) connected to the voltage source are NOT also coupled to an output stage.

In view of the foregoing remarks, Applicant respectfully submits that the rejection of claims 1-4 and 14 has been overcome. Applicant respectfully requests that the rejection of these claims be withdrawn and that a notice of allowance be forthcoming at the Examiner's earliest convenience.

***Allowed and Allowable Claims***

Applicant notes with appreciation that claims 10-13 are allowed and that claim 15 is allowable if rewritten in independent form. As claim 14, from which claim 15 depends, is believed to be patentably distinct, Applicant respectfully declines to amend claim 15 to place it in independent form. Applicant, however, reserves the right to make such an amendment in the unfortunate event that the rejection of claim 14 is maintained.

A Notice of Allowability of claims 1-15 is now eagerly awaited at the Examiner's first convenience. The undersigned may be contacted if there are any questions about this filing.

Respectfully submitted,



Renee' Michelle Larson  
Registration No. 36,193  
Larson and Associates, P.C.  
221 East Church Street  
Frederick, MD 21701  
Phone (301) 668-3073  
Fax (301) 668-3074

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